#### **Exploring Emerging Technologies in the Extreme** Scale HPC Co-Design Space with **Holistic Performance Modeling**

Jeffrey S. Vetter Jeremy Meredith

Presented to Exascale Applications and Software Conference (EASC)

EPCC/University of Edinburgh

22 Apr 2015

OAK RIDGE NATIONAL LABORATORY

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S B	alvenie 30 YO anff 1976 (CC)	34	40.0%	£10.90		C	Glen Scotia 18 YO	18	46.0%	£7.50 £4.90
HB	en Nevis 10 YO	10	46.0%	£3.90 £4.00		CC	Glen Scotia 12 YO Glen Scotia Cask Strength	15	59.9%	£5.80
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	more Tempest more Original	10	40.0%	£5.50		S	Glenfarclas 105 (CS)	10	60.0% 43.0%	£5.90 £9.00
Bow	more 18 YO	18	43.0%	£9.50 £7.90		S	Glenfarclas 21 YO Glenfiddich 12 YO	12	40.0%	£4.90
	more Darkest more 25 YO	15 25	40.0%	£35.00		S	Glenfiddich 18 YO	18	40.0%	£12.00
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I Laphrolag Triple Wood IS Ledaig 10 YO	NI 10		3% 1	26.90 24.00		HIS	Teaninich (CC) Tobermory			10	16.3%	£4.50
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Chapman & Hall/CRC Computational Science Series

Contemporary High Performance Computing From Petascale toward Exascale VOLUME TWO

Edited by Jeffrey S. Vetter



National Laborator

## **Overview**

- Our community has major challenges in HPC as we move to extreme scale
  - Power, Performance, Resilience, Productivity
  - Major shifts in architectures, software, applications
    - Not just HPC: Most uncertainty in two decades
- New technologies emerging to address some of these challenges
  - Heterogeneous computing
  - Nonvolatile memory
- Consequently, we now have critical situations in
  - Portable programming models
  - Performance prediction for procurement, optimization, etc
- Aspen is a tool we have developed for performance prediction <u>\*OAK</u>

# Surveying the HPC Landscape: Today and Tomorrow

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#### **Notional Exascale Architecture Targets** (From Exascale Arch Report 2009)

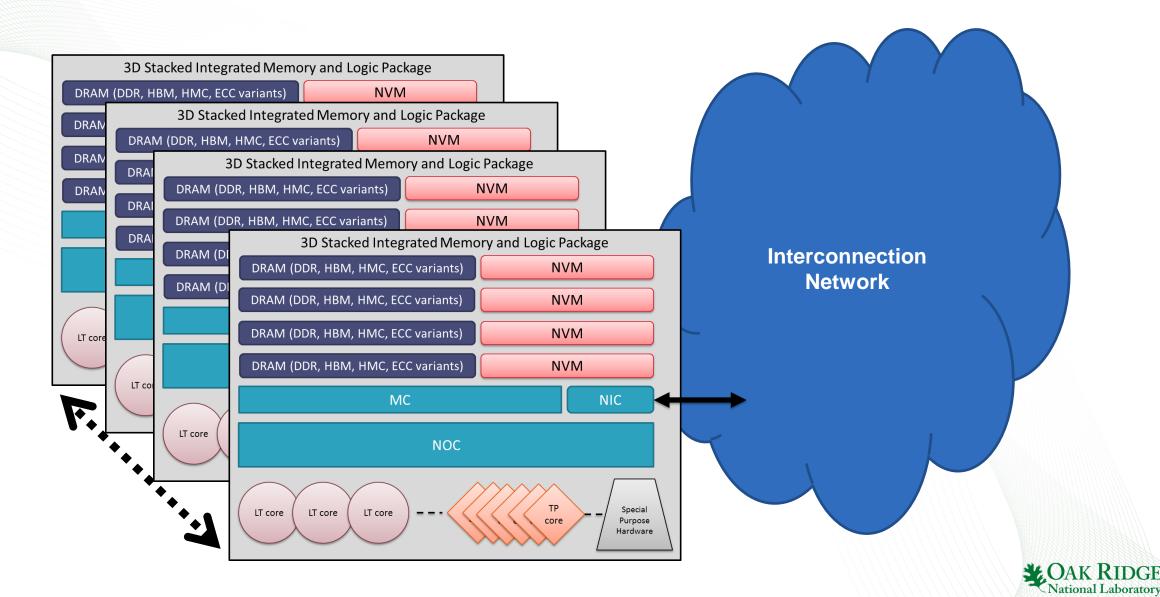
System attributes	2001	2010	"2	015"	"2018"		
System peak	10 Tera	2 Peta	200 Pe	taflop/sec	1 Exaflop/sec		
Power	~0.8 MW	6 MW	15	MW	20 MW		
System memory	0.006 PB	0.3 PB	5	РВ	32-64 PB		
Node performance	0.024 TF	0.125 TF	0.5 TF	7 TF	1 TF	10 TF	
Node memory BW		25 GB/s	0.1 TB/sec	1 TB/sec	0.4 TB/sec	4 TB/sec	
Node concurrency	16	12	O(100)	O(1,000)	O(1,000)	O(10,000)	
System size (nodes)	416	18,700	50,000	5,000	1,000,000	100,000	
Total Node Interconnect BW		1.5 GB/s	150 GB/sec	1 TB/sec	250 GB/sec	2 TB/sec	
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Parallel I/O ??

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http://science.energy.gov/ascr/news-and-resources/workshops-and-conferences/grand-challenges/

### **Notional Future Architecture**

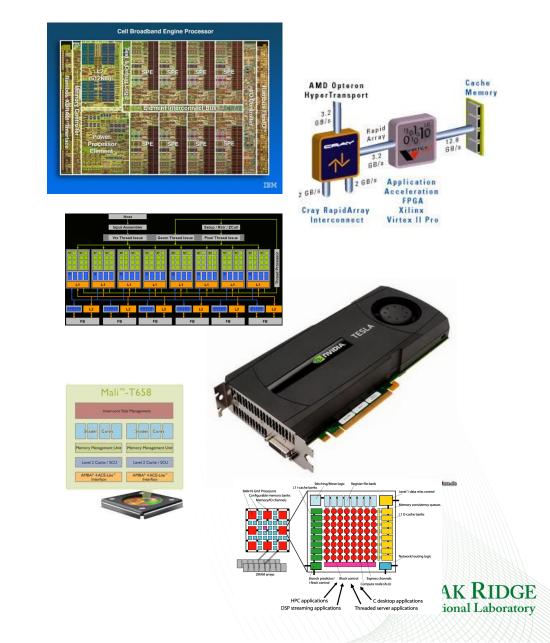


# **Earlier Experimental Computing Systems**

~2004

<sup>o</sup>opular architectures since

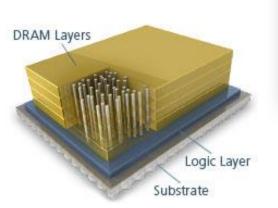
- The past decade has started the trend away from traditional 'simple' architectures
- Mainly driven by facilities costs and successful (sometimes heroic) application examples
- Examples
  - Cell, GPUs, FPGAs, SoCs, etc
- Many open questions
  - Understand technology challenges
  - Evaluate and prepare applications
  - Recognize, prepare, enhance programming models

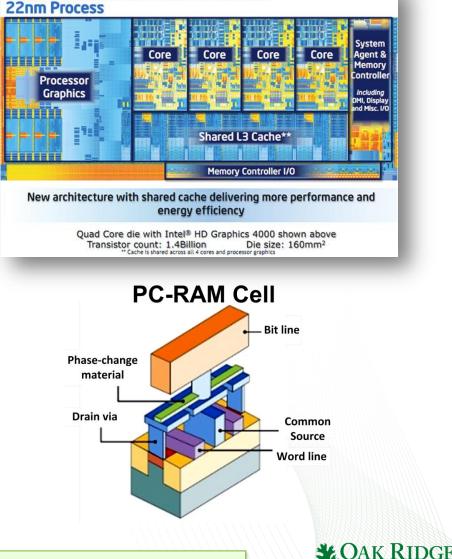


# **Emerging Computing Architectures – Future**

#### Heterogeneous processing

- Latency tolerant cores
- Throughput cores
- Special purpose hardware (e.g., AES, MPEG, RND)
- Fused, configurable memory
- Memory
  - 2.5D and 3D Stacking
  - HMC, HBM, WIDEIO2, LPDDR4, etc
  - New devices (PCRAM, ReRAM)
- Interconnects
  - Collective offload
  - Scalable topologies
- Storage
  - Active storage
  - Non-traditional storage architectures (key-value stores)
- Improving performance and programmability in face of increasing complexity
  - Power, resilience





National Laboratory

3rd Generation Intel<sup>®</sup> Core<sup>™</sup> Processor:

HPC (mobile, enterprise, embedded) computer design is more fluid now than in the past two decades.

### **Recent announcements**

#### Nvidia and IBM create GPU interconnect for faster supercomputing

"NVLink" shares up to 80GB of data per second between CPUs and GPUs

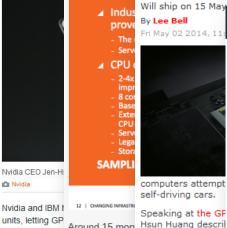
#### by Jon Brodkin - M It Begins: AMD Announces Its First ARM Based Server SoC, 64-bit/8-core Opteron All00

by Anand Lal Shimpi on January 28, 2014 6:35 PM EST

Posted in CPUs IT Computing Enterprise enterprise CPUs AMD Opteron Opteron A1100 ARM

"SEATTLE" 64 DIT ADM CEDVED DROCESCOD

FIRST 28NM AR Nvidia Jetson TK1 mini supercomputer is up for pre-order



Around 15 mon The fatter pipe can run, but at a sl compared to 16 2014. Less than

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PRESS RELEASE

MarketWatch

#### Altera and IBM Unveil **FPGA-accelerated POWER** Systems with Coherent Shared Memory

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Published: Nov 17, 2014 8:00 a.m. ET

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POWER8 Systems that Leverage Reprogrammable FPGA Accelerators Gain Significant Improvements in System Performance, Efficiency and Flexibility

NEW ORLEANS, Nov. 17, 2014 /PRNewswire/ -- SuperComputing 2014 -- Altera Corporation ALTR, +0.00% and IBM IBM, +0.00% today unveiled the industry's first FPGA-based acceleration platform that coherently connects an FPGA to a POWER8 CPU leveraging IBM's Coherent Accelerator Processor Interface (CAPI). The reconfigurable hardware accelerator features shared virtual memory between the FPGA and processor which significantly improves system performance, efficiency and flexibility in high-performance computing (HPC) and data center applications. Altera and IBM are presenting several POWER8 systems that are coherently accelerated using FPGAs at SuperComputing 2014.

#### Intel's 14nm Broadwell GPU takes shape, indicates major improvements over Haswell

By Sebastian Anthony on November 5, 2013 at 10:21 am | 16 Comments



(intel) inside

seriously as a means of accelerating applications and has crafted a hybrid chip that marries an FPGA to a Xeon E5 processor and puts them in the same processor socket

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#### NVRAM Technology Continues to Improve – Driven by Market Forces





#### designlines MEMORY

#### News & Analysis 3D NAND Production Starts at Samsung

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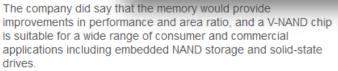
Peter Clarke 8/6/2013 08:05 AM EDT 16 comments

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LONDON — Samsung production of a 128 G multiple layers, and cli

The memory is based conventional floating ( In the vertical arrange reliability between a fa conventional floating-( in a press release.

The technology is cap did not disclose how n vertical NAND, nor whe whether it had relaxed in 2D memory, which s



The V-NAND component has the same memory capacity as a 128

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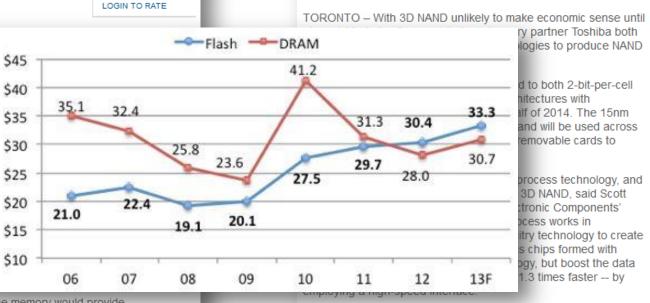
#### News & Analysis 3D NAND Transition: 15nm Process Technology Takes Shape

Gary Hilson	
5/13/2014 08:15 AM EDT	
5 comments	

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Nelson said there is room to advance floating gates before moving

http://www.eetasia.com/STATIC/ARTICLE\_IMAGES/201212/EEOL\_20 12DEC28\_STOR\_MFG\_NT\_01.jpg

Original URL: http://www.theregister.

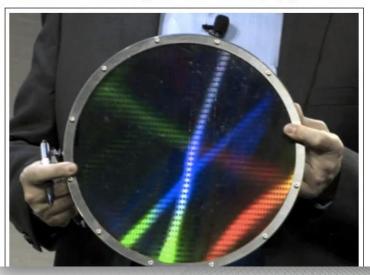
HP 100TB Memristor drives Universal memory slow in com By Chris Mellor

Posted in Storage, 1st November 2013 02:28 GMT

Blocks and Files HP has warned *El Reg* not to get its hopes up too high after the tech titan's CTO Martin Fink suggested StoreServ arrays could be packed with 100TB Memristor drives come 2018.

In five years, according to Fink, DRAM and NAND scaling will hit a wall, limiting the maximum capacity of the technologies: process shrinks will come to a shuddering halt when the memories' reliability drops off a cliff as a side effect of reducing the size of electronics on the silicon dies.

The HP answer to this scaling wall is Memristor, its flavour of resistive RAM technology that is supposed to have DRAM-like speed and better-than-NAND storage density. Fink claimed at an HP Discover event in Las Vegas that Memristor devices will be ready by the time flash NAND hits its limit in five years. He also showed off a Memristor wafer, adding that it could have a 1.5PB capacity by the end of the decade.



### **Comparison of emerging memory technologies**

	SRAM	DRAM	eDRAM	2D NAND Flash	3D NAND Flash	PCRAM	STTRAM	2D ReRAM	3D ReRAM
Data Retention	N	Ν	N	Y	Y	Y	Y	Y	Y
Cell Size (F <sup>2</sup> )	50-200	4-6	19-26	2-5	<1	4-10	8-40	4	<1
Minimum F demonstrated (nm)	14	25	22	16	64	20	28	27	24
Read Time (ns)	< 1	30	5	104	104	10-50	3-10	10-50	10-50
Write Time (ns)	< 1	50	5	10 <sup>5</sup>	105	100-300	3-10	10-50	10-50
Number of Rewrites	1016	1016	1016	10 <sup>4</sup> -10 <sup>5</sup>	10 <sup>4</sup> -10 <sup>5</sup>	10 <sup>8</sup> -10 <sup>10</sup>	1015	10 <sup>8</sup> -10 <sup>12</sup>	10 <sup>8</sup> -10 <sup>12</sup>
Read Power	Low	Low	Low	High	High	Low	Medium	Medium	Medium
Write Power	Low	Low	Low	High	High	High	Medium	Medium	Medium
Power (other than R/W)	Leakage	Refresh	Refresh	None	None	None	None	Sneak	Sneak
Maturity									



# Thinking back to 2009 projections, where is DOE in 2015?

System attributes	Toda	ay	CORAL				
Name	TITAN	MIRA	Summit	Aurora			
System peak (PF)	27	10	150	180			
Peak Power (MW)	9	4.8	10	13			
Total system memory	710TB	768TB	2 PB DDR4 + HBM + 2.7 PB persistent memory	>7 PB High Bandwidth On-Package Memory, local Memory and Persistent Memory			
Node performance (TF)	1.452	0.204	> 40	> 17 times Mira			
Node processors	AMD Opteron Nvidia Kepler	64-bit PowerPC A2	Multiple IBM Power9 CPUs & multiple Nvidia Voltas GPUS	Intel Xeon Phi processors (codenamed Knights Hill)			
System size (nodes)	18,688 nodes	49,152	>3,400 nodes	>50,000 nodes			
System Interconnect	Gemini	5D Torus	Dual Rail EDR-IB	2nd generation Intel Omni-Path Architecture			
File System	32 PB 1 TB/s, Lustre®	26 PB 300 GB/s GPFS™	120 PB 1 TB/s GPFS™	150 PB >1 TB/s Lustre <sup>®</sup>			



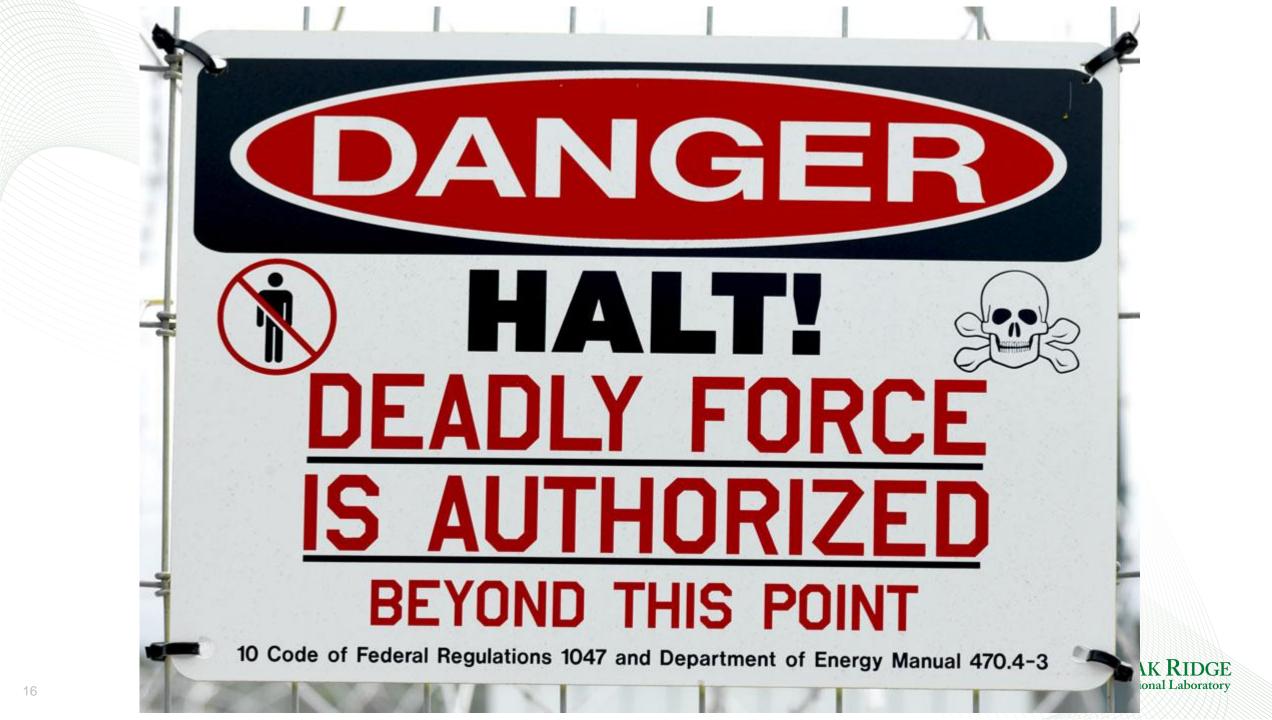
### Some ratios will be challenging to mitigate

System attributes	2001	2010	2014	"2015	. <i>"</i> "	est 2018	Ratio of Summit to Titan	"2018	8"
Name	Seaborg3	Jaguar	Titan			SUMMIT			
System peak	10 Tera	2 Peta	27	200		136	5.04	1 Exaflop/sec	
Power (MW)	0.8	6	9	15		10	1.11	20	
Node main memory (GB)			38			512	13.47		
System memory (PB)	0.006	0.3	0.7106	5		1.7408	2.45	32-6	64
Node Persistent Memory (GB)						800			
System Persistent Memory (PB)						2.72	8		
Node performance (TF)	0.024	0.125	1.4	0.5	7	40	28.57	1	10
Node memory BW		25 GB/s		0.1 TB/sec	1 TB/sec			0.4 TB/sec	4 TB/sec
Node concurrency	16	12		O(100)	O(1,000)	*POWER9s + *VOLTAs		O(1,000)	O(10,000)
System size (nodes)	416	18700	18700	50000	5000	3400	0.18	1000000	100000
Total Node Interconnect BW		1.5 GB/s		150 GB/sec	1 TB/sec			250 GB/sec	2 TB/sec
injection bandwidth per node (GB/s)			6.4			23	3.59		
File system capacity (PB)			32			120	3.75		
File system bandwidth (TB/s)			1			1	1.00		
MTTI		day		O(1 day)				O(1 day)	

#### **Observations about these trends**

Aside from all the interesting technical questions for computer scientists...





### **Observations about these trends (2)**

- 1. For the success of HPC, we need to be very careful at this point
- 2. Complexity is everyone's enemy!

- 3. Performance portable programming models should be mandatory on all current and future architectures
  - 1. Increasingly, apps teams are spending time porting to new architectures rather than doing science
- 4. Performance prediction techniques and tools are critical
  - Previously, a poor (procurement, optimization, facility) decision could cost 30%; now it could be 10x!
- 5. And then there is power consumption, reliability, etc



#### Holistic Performance Modeling for Extreme-Scale HPC



### **Prediction Techniques Ranked**

	Speed	Ease	Flexibility	Accuracy	Scalability	_
Ad-hoc Analytical Models	1	3	2	4	1	-
Structured Analytical Models	1	2	1	4	1	
Simulation – Functional	3	2	2	3	3	
Simulation – Cycle Accurate	4	2	2	2	4	
Hardware Emulation (FPGA)	3	3	3	2	3	
Similar hardware measurement	2	1	4	2	2	
Node Prototype	2	1	4	1	4	
Prototype at Scale	2	1	4	1	2	
Final System	-	-	-	-	-	



### **Prediction Techniques Ranked**

	Speed	Ease	Flexibility	Accuracy	Scalability
Ad-hoc Analytical Models	1	3	2	4	1
Structured Analytical Models	1	2	1	4	1
Aspen	1	1	1	4	1
Simulation – Functional	3	2	2	3	3
Simulation – Cycle Accurate	4	2	2	2	4
Hardware Emulation (FPGA)	3	3	3	2	3
Similar hardware measurement	2	1	4	2	2
Node Prototype	2	1	4	1	4
Prototype at Scale	2	1	4	1	2
Final System	-	-	-	-	-
2					

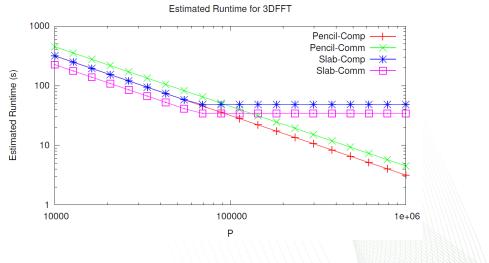


#### **Aspen – Design Goals**

Abstract Scalable Performance Engineering Notation

- Create a deployable, extensible, and highly semantic representation for analytical performance models
- Design and implement a new language for analytical performance modeling
- Use the language to create machine-independent models for important applications and kernels
- Models are composable

Listing 2. Aspen statements for the local 1D FFTs



K. Spafford and J.S. Vetter, "Aspen: A Domain Specific Language for Performance Modeling," in SC12: ACM/IEEE International Conference for High Performance Computing, Networking, Storage, and Analysis, 2012

22

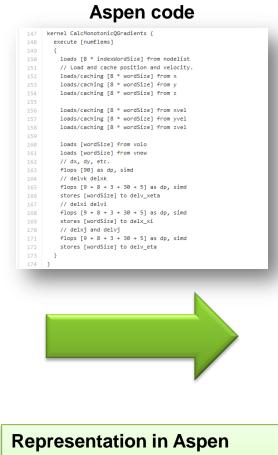
# **Aspen Design Flow**

#### Source code

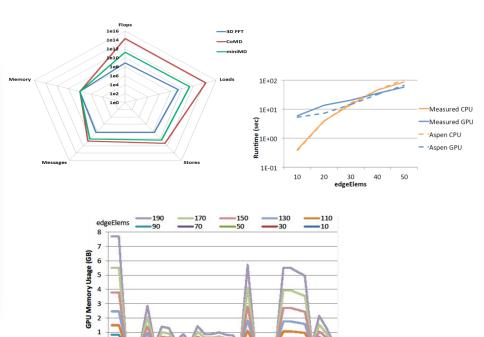
2324	static inline
2325	<pre>void CalcMonotonicQGradientsForElems(Index t p nodelist[T NUMELEM8],</pre>
2326	Real t p x[T_NUMNODE], Real t p y[T_NUMNODE], Real t p_z[T_NUMNODE],
2327	Real t p xd[T NUMNODE], Real t p yd[T NUMNODE], Real t p zd[T NUMNODE],
2328	Real t p volo[T NUMELEM], Real t p vnew[T NUMELEM],
2329	Real t p delx zeta[T NUMELEM], Real t p delv zeta[T NUMELEM],
2330	Real t p delx xi [T NUMELEM], Real t p delv xi [T NUMELEM],
2331	Real t p delx eta[T NUMELEM], Real t p delv eta[T NUMELEM])
2332	白 (
2333	Index_t i;
2334	<pre>Index_t numElem = m_numElem;</pre>
2335	<pre>#pragma acc parallel loop independent present(p_vnew, p_nodelist, p_x, p_y, p_z, p_xd,</pre>
2336	p_yd, p_zd, p_volo, p_delx_xi, p_delx_eta, p_delx_zeta, p_delv_xi, p_delv_eta,\
2337	p_delv_zeta)
2338	<pre>for (i = 0 ; i &lt; numElem ; ++i ) {</pre>
2339	<pre>const Real_t ptiny = 1.e-36 ;</pre>
2340	Real_t ax,ay,az ;
2341	Real_t dxv,dyv,dzv ;
2342	
2343	<pre>const Index_t *elemToNode = &amp;p_nodelist[8*i];</pre>
2344	<pre>Index_t n0 = elemToNode[0] ;</pre>
2345	<pre>Index_t n1 = elemToNode[1] ;</pre>
2346	<pre>Index_t n2 = elemToNode[2] ;</pre>
2347	<pre>Index_t n3 = elemToNode[3] ;</pre>
2348	<pre>Index_t n4 = elemToNode[4] ;</pre>
2349	<pre>Index_t n5 = elemToNode[5] ;</pre>
2350	<pre>Index_t n6 = elemToNode[6] ;</pre>
2351	<pre>Index_t n7 = elemToNode[7] ;</pre>
2352	
2353	Real_t x0 = p_x[n0] ;

#### **Creation**

- Manual for future applications
- Static analysis via compilers
- Historical
- Empirical



- Modular
- Sharable
- Composable
- Reflects prog structure
- Existing models for MD, UHPC CP 1, Lulesh, 3D FFT, CoMD, VPFFT, ...



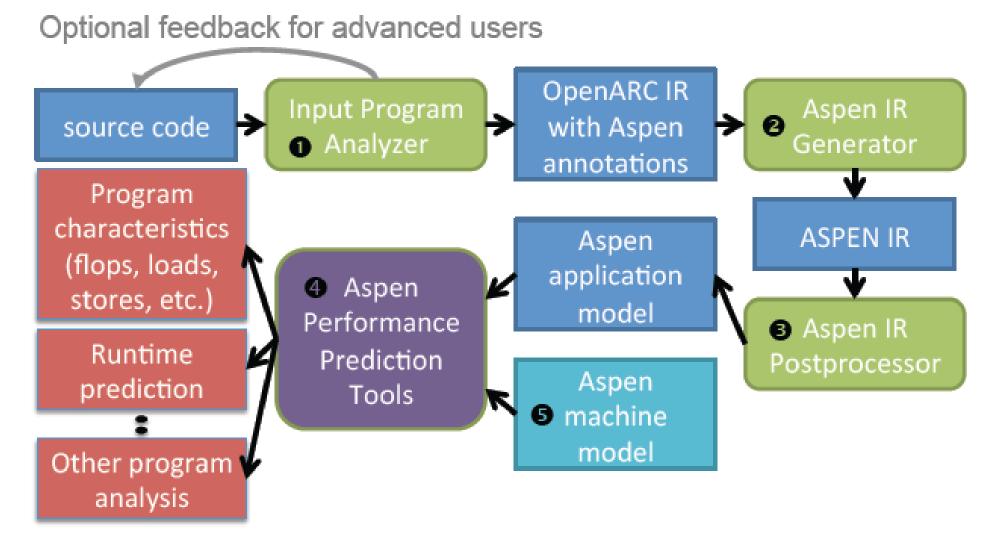
#### <u>Use</u>

- Interactive tools for graphs, queries
- Design space optimization
- Drive simulators
- Feedback to runtime systems



K.2Spafford and J.S. Vetter, "Aspen: A Domain Specific Language for Performance Modeling," in SC12: ACM/IEEE International Conference for High Performance Computing, Networking, Storage, and Analysis, 2012

### **Creating Aspen Models**



S. Lee, J.S. Meredith, and J.S. Vetter, "COMPASS: A Framework for Automated Performance Modeling and Prediction," in ACM International Conference on Supercomputing (ICS). Newport Beach, California: ACM, 2015, 10.1145/2751205.2751220.



# Simple MM example generated from COMPASS

```
int N = 1024;
 1
     void matmul(float *a, float *b, float *c){ int i, j, k ;
 \mathbf{2}
     \#pragma acc kernels loop gang copyout(a[0:(N*N)]) \
 3
     copyin(b[0:(N*N)],c[0:(N*N)])
 4
      for (i=0; i<N; i++)
 \mathbf{5}
     #pragma acc loop worker
 6
 \overline{7}
        for (j=0; j<N; j++) { float sum = 0.0;
         for (k=0; k<N; k++) {sum+=b[i*N+k]*c[k*N+j];}
         a[i*N+j] = sum; \}
      } //end of i loop
     } //end of matmul()
     int main() {
      int i; float *A = (float*) malloc(N*N*sizeof(float));
      float *B = (float*) malloc(N*N*sizeof(float));
      float *C = (float*) malloc(N*N*sizeof(float));
      for (i = 0; i < N*N; i++)
       \{ A[i] = 0.0F; B[i] = (float) i; C[i] = 1.0F; \}
     #pragma aspen modelregion label(MM)
      matmul(A,B,C);
      free(A); free(B); free(C); return 0;
     } //end of main()
21
```

1	model MM {
$^{2}$	param floatS = 4; param N = $1024$
3	data A as Array((N*N), floatS)
4	data B as Array((N*N), floatS)
5	data C as Array((N*N), floatS)
6	kernel matmul {
7	execute matmul2_intracommIN
8	{ intracomm [floatS*(N*N)] to C as copyin
9	intracomm [floatS*(N*N)] to B as copyin }
10	map matmul2 [N] {
11	map matmul3 [N] {
12	iterate [N] {
13	execute matmul5
14	$\{ \text{ loads [floatS] from B as stride}(1) \}$
15	loads [floatS] from C; flops [2] as sp, simd }
16	} //end of iterate
17	execute matmul6 { stores [floatS] to A as $stride(1)$ }
18	} // end of map matmul3
19	} //end of map matmul2
20	execute matmul2_intracommOUT
21	$\{ intracomm [floatS*(N*N)] to A as copyout \}$
22	} //end of kernel matmul
23	kernel main { matmul() }
24	} //end of model MM



### **LULESH** in Aspen

branch: master      aspen / models / lulesh / lulesh.aspen		⊞ 🚯		
jsmeredith on Sep 20, 2013 adding models			14	
1 contributor		14	9	
		15	0	
336 lines (288 sloc) 9.213 kb 🛛 🖉 🧨 📺				
		15	2	
1 //		15		
2 // lulesh.aspen			-	
3 // 4 // An ASPEN application model for the LULESH 1.01 challenge problem. Based			4	
4 // An ASELW appreciation model for the collisin 1.01 charlenge problem. Based 5 // on the CUDA version of the source code found at:		15	5	
6 // https://computation.llnl.gov/casc/ShockHydro/			6	
7 //		15	7	
<pre>8 param nTimeSteps = 1495</pre>		15	8	
9		15	0	
10 // Information about domain		16		
11 param edgeElems = 45			-	
12 param edgeNodes = edgeElems + 1 13		16	1	
14 param numElems = edgeElems^3		16	2	
15 param numNodes = edgeNodes^3			3	
16		16	4	
17 // Double precision			5	
18 param wordSize = 8				
19		16		
20 // Element data			7	
21 data mNodeList as Array(numElems, wordSize) 22 data mMatElemList as Array(numElems, wordSize)			8	
22 data mMatElemList as Array(numElems, wordSize) 23 data mNodeList as Array(8 * numElems, wordSize) // 8 nodes per element			9	
24 data mixim as Array(numElems, wordSize)			0	
25 data mlxip as Array(numElems, wordSize)			1	
26 data mletam as Array(numElems, wordSize)				
27 data mletap as Array(numElems, wordSize)			2	
28 data mzetam as Array(numElems, wordSize)			3	
29 data mzetap as Array(numElems, wordSize)			4 }	
30 data melemBC as Array(numElems, wordSize) 31 data mE as Array(numElems, wordSize)				
31 data mE as Array(numElems, wordSize) 32 data mP as Array(numElems, wordSize)				



## **LULESH – runtime optimizations**

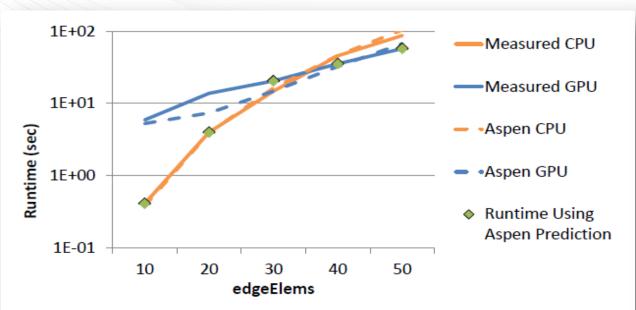


Fig. 7: Measured and predicted runtime of the entire LULESH program on CPU and GPU, including measured runtimes using the automatically predicted optimal target device at each size.

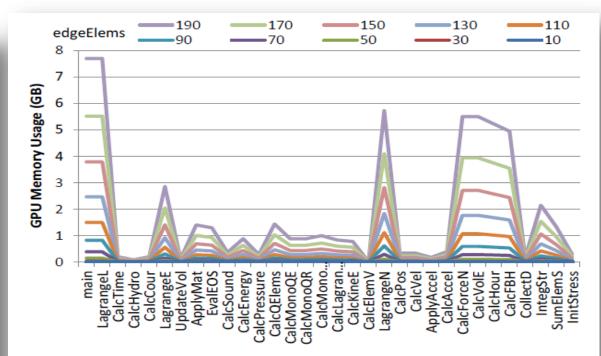


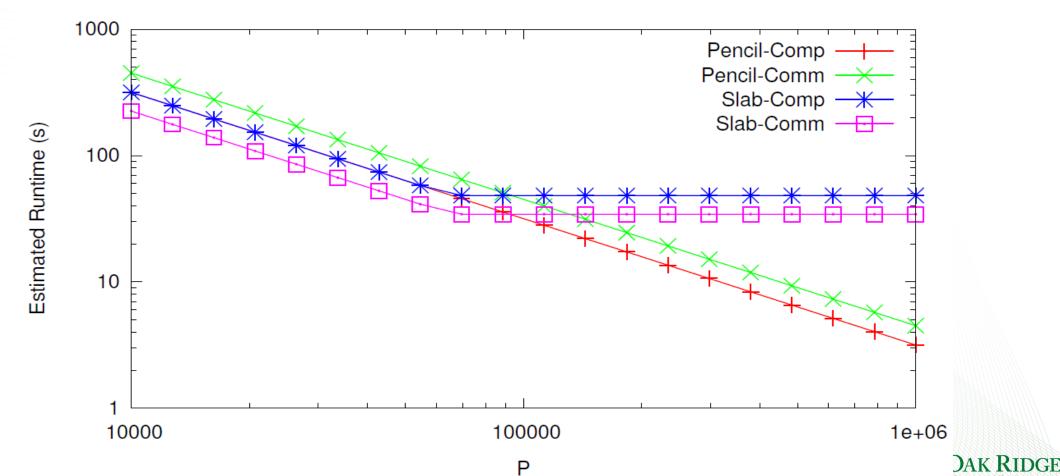
Fig. 8: GPU Memory Usage of each Function in LULESH, where the memory usage of a function is inclusive; value for a parent function includes data accessed by its child functions in the call graph.



3DFFT	<pre>// Dimension of cubic 3D Volume param n = 8192 param a = 6.3 param wordSize = 16 // Double Complex Words param dataPerProc = (n^3 * wordSize) / P data fftVolume [n^3 * wordSize]</pre>
<pre>control pencil {    localFFT -&gt; transpose    exchange    localFFT -&gt; transpose    exchange    localFFT -&gt; transpose }</pre>	<pre>// in Y localFFT -&gt; transpose // in X // in Y localFFT -&gt; transpose // in Y exchange</pre>
<pre>kernel localFFT {     exposes parallelism [n^     requires flops [5 * n *     requires loads [a * (n*         from fftVolume }</pre>	
<pre>kernel exchange {     exposes parallelism [H     requires messages [(n'         allToAll }</pre>	P] ^3 * wordSize) / P] as

#### **3DFFT: Slab vs. Pencil Tradeoff** Ideal Parallelism

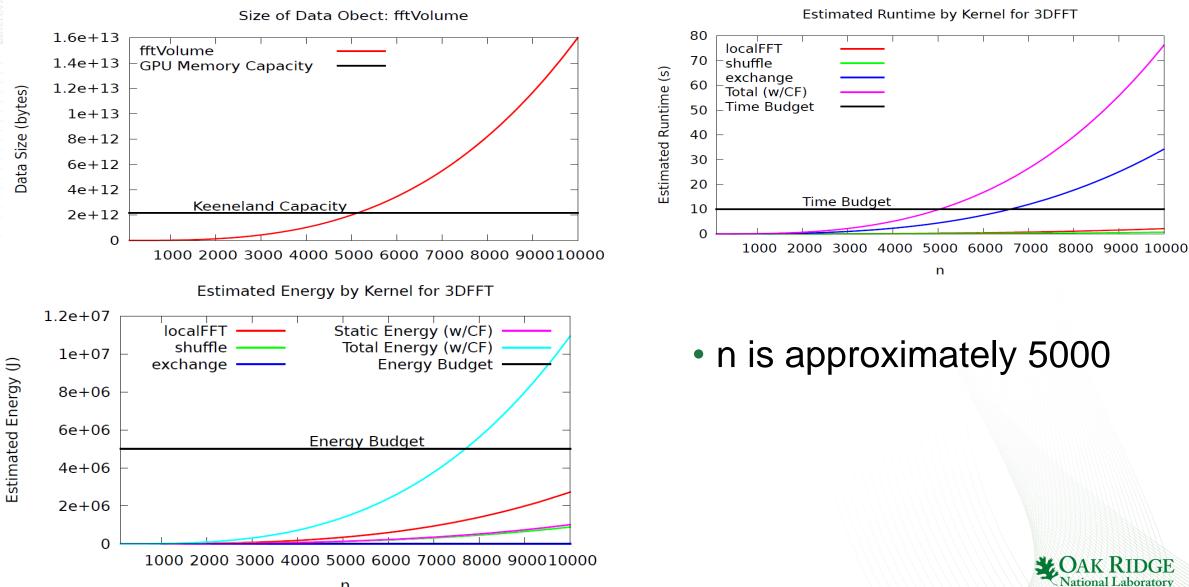
Insights become obvious with Aspen



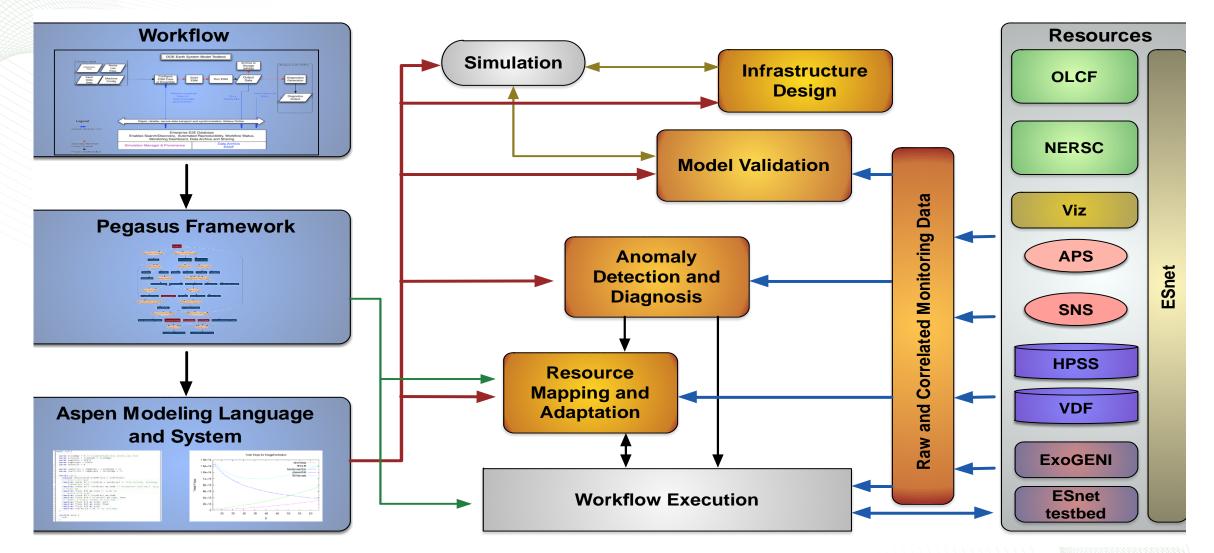
Jational Laboratory

Estimated Runtime for 3DFFT

#### **Design Space Exploration**



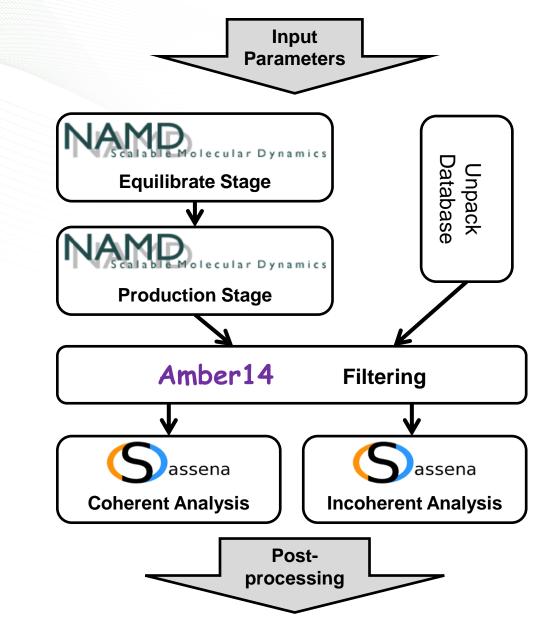
#### **PANORAMA Overview**



E. Deelman, C. Carothers et al., "PANORAMA: An Approach to Performance Modeling and Diagnosis of Extreme Scale Workflows," International Journal of High Performance Computing Applications, (to appear), 2015,



#### **Spallation Neutron Source Workflow**



```
kernel main
{
   par {
      seq {
         call namd_eq_200()
         call namd_prod_200()
      seq {
         call namd_eq_290()
         call amd_prod_290()
      call unpack_database()
   }
   par
           amber_ptraj_200()
      call
           amber_ptraj_290()
      call
   par
      call sassena_coh_200()
      call sassena_coh_290()
      call sassena_inc_200()
      call sassena_inc_290()
   }
                         🕊 OAK RIDGE
                          National Laboratory
}
```

# Summary

- Our community has major challenges in HPC as we move to extreme scale
  - Power, Performance, Resilience, Productivity
  - Major shifts in architectures, software, applications
    - Not just HPC: Most uncertainty in two decades
- New technologies emerging to address some of these challenges
  - Heterogeneous computing
  - Nonvolatile memory
- Consequently, we now have critical situations in
  - Portable programming models
  - Performance prediction for procurement, optimization, etc
- Aspen is a tool we have developed for performance prediction <u>\*OAK</u>

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- Contributors and Sponsors
  - Future Technologies Group: http://ft.ornl.gov
  - US Department of Energy Office of Science
    - DOE Vancouver Project: <u>https://ft.ornl.gov/trac/vancouver</u>
    - DOE Blackcomb Project: <u>https://ft.ornl.gov/trac/blackcomb</u>
    - DOE ExMatEx Codesign Center: <u>http://codesign.lanl.gov</u>
    - DOE Cesar Codesign Center: <u>http://cesar.mcs.anl.gov/</u>
    - DOE Exascale Efforts: <u>http://science.energy.gov/ascr/research/computer-science/</u>
  - Scalable Heterogeneous Computing Benchmark team: <u>http://bit.ly/shocmarx</u>
  - US National Science Foundation Keeneland Project: <u>http://keeneland.gatech.edu</u>
  - US DARPA
  - NVIDIA CUDA Center of Excellence



